NEO FORZA DDR5 32GB-5200 / 5600 / 6000 / 6400 RGB UDIMM

General Description

This chapter gives an overview of the 288–pin DDR5 unbuffered dual in-line memory modules product family and describes its main characteristics.

Features

- 288-Pin RGB UDIMM (Lead-Free) DDR5 SDRAM Memory Module.
- Data transfer rates: PC5-41600 / 44800 / 48000 / 51200.
- Power supply: VDD: 1.067V ~ 1.166V.
  XMP VDD: 5200@1.1V / 5600 @1.2V / 6000MHz @1.3V / 6400MHz @1.4V
- Module organization: 4096Meg × 64.
- DRAM organization: 2048Mb × 8.
- 32 internal banks; 8 groups of 4 banks each.
- 16-bit prefetch.
- BL16, BC8 OTF, BL32, BL32 OTF supported.
- DFE (Decision Feedback Equalization) for DQ.
- On-Die ECC.
- Same Bank Refresh.
- On Die Termination(ODT) via Mode Register setting.
- Connectivity Test (CT)

Ordering Information for Compliant Products

Part Number	Compliance Code	Number of Ranks	DRAM Organisation	# of SDRAMs
NMGD532F82-5200JI20	32GB / XMP PC5-41600 / 40-40-40	2	2Gb x8	16
NMGD532F82-5600EI20	32GB / XMP PC5-44800 / 40-40-40	2	2Gb x8	16
NMGD532F82-6000LI20	32GB / XMP PC5-48000 / 40-40-40	2	2Gb x8	16
NMGD532F82-6400FI20	32GB / XMP PC5-51200 / 40-40-40	2	2Gb x8	16

Pin Assignments

288-Pin DDR5 UDIMM Front								288-Pin DDR5 UDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VIN_BULK	37	DQ20_A	73	CK0_A_c	109	V_{SS}	145	VIN_BULK	181	DQ22_A	217	CK1_A_c	253	V_{SS}
2	RFU	38	V_{SS}	74	V_{SS}	110	DQ5_B	146	VIN_BULK	182	V_{SS}	218	V_{SS}	254	DQ7_B
3	RFU	39	DQ21_A	75	RFU	111	V_{SS}	147	PWR_-GOOD	183	DQ23_A	219	RFU	255	V_{SS}
4	HSCL	40	V_{SS}	76	RFU	112	DQ8_B	148	HSA	184	V_{SS}	220	RFU	256	DQ10_B
5	HSDA	41	DQ24_A	77	V_{SS}	113	V_{SS}	149	RFU	185	DQ26_A	221	V_{SS}	257	V_{SS}
6	V_{SS}	42	V_{SS}	78	CK0_B_t	114	DQ9_B	150	V_{SS}	186	V_{SS}	222	CK1_B_t	258	DQ11_B
7	RFU	43	DQ25_A	79	CK0_B_c	115	V_{SS}	151	PWR_EN	187	DQ27_A	223	CK1_B_c	259	V_{SS}
8	V_{SS}	44	V_{SS}	80	V_{SS}	116	DM1_B_n	152	RFU	188	V_{SS}	224	V_{SS}	260	DQS1_B_c
9	DQ0_A	45	DM3_A_n	81	RFU	117	V_{SS}	153	V_{SS}	189	DQS3_A_c	225	RFU	261	DQS1_B_t
10	V_{SS}	46	V_{SS}	82	CA12_B	118	DQ12_B	154	DQ2_A	190	DQS3_A_t	226	RFU	262	V_{SS}
11	DQ1_A	47	DQ28_A	83	V_{SS}	119	V_{SS}	155	V_{SS}	191	V_{SS}	227	V_{SS}	263	DQ14_B
12	V_{SS}	48	V_{SS}	84	CA10_B	120	DQ13_B	156	DQ3_A	192	DQ30_A	228	CA11_B	264	V_{SS}
13	DQS0_A_c	49	DQ29_A	85	CA8_B	121	V_{SS}	157	V_{SS}	193	V_{SS}	229	CA9_B	265	DQ15_B
14	DQS0_A_t	50	V_{SS}	86	V_{SS}	122	DQ16_B	158	DM0_A_n	194	DQ31_A	230	V_{SS}	266	V_{SS}
15	V_{SS}	51	CB0_A	87	CA6_B	123	V_{SS}	159	V_{SS}	195	V_{SS}	231	CA7_B	267	DQ18_B
16	DQ4_A	52	V_{SS}	88	CA4_B	124	DQ17_B	160	DQ6_A	196	CB2_A	232	CA5_B	268	V_{SS}
17	V_{SS}	53	CB1_A	89	V_{SS}	125	V_{SS}	161	V_{SS}	197	V_{SS}	233	V_{SS}	269	DQ19_B
18	DQ5_A	54	V_{SS}	90	CA2_B	126	DQS2_B_c	162	DQ7_A	198	CB3_A	234	CA3_B	270	V_{SS}
19	V_{SS}	55	DQS4_A_c	91	CA0_B	127	DQS2_B_t	163	V_{SS}	199	V_{SS}	235	CA1_B	271	DM2_B_n
20	DQ8_A	56	DQS4_A_t	92	V_{SS}	128	V_{SS}	164	DQ10_A	200	ALERT_n	236	V_{SS}	272	V_{SS}
21	V_{SS}	57	V_{SS}	93	CS0_B_n	129	DQ20_B	165	V_{SS}	201	V_{SS}	237	CS1_B_n	273	DQ22_B
22	DQ9_A	58	CS0_A_n	94	V_{SS}	130	V_{SS}	166	DQ11_A	202	CS1_A_n	238	V_{SS}	274	V_{SS}
23	V_{SS}	59	V_{SS}	95	RESET_n	131	DQ21_B	167	V_{SS}	203	V_{SS}	239	DQS4_B_c	275	DQ23_B
24	DM1_A_n	60	CA0_A	96	V_{SS}	132	V_{SS}	168	DQS1_A_c	204	CA1_A	240	DQS4_B_t	276	V_{SS}
25	V_{SS}	61	CA2_A	97	CB0_B	133	DQ24_B	169	DQS1_A_t	205	CA3_A	241	V_{SS}	277	DQ26_B
26	DQ12_A	62	V_{SS}	98	V_{SS}	134	V_{SS}	170	V_{SS}	206	V_{SS}	242	CB2_B	278	V_{SS}
27	V_{SS}	63	CA4_A	99	CB1_B	135	DQ25_B	171	DQ14_A	207	CA5_A	243	V_{SS}	279	DQ27_B
28	DQ13_A	64	CA6_A	100	V_{SS}	136	V_{SS}	172	V_{SS}	208	CA7_A	244	CB3_B	280	V_{SS}
29	V_{SS}	65	V_{SS}	101	DQ0_B	137	DM3_B_n	173	DQ15_A	209	V_{SS}	245	V_{SS}	281	DQS3_B_c
30	DQ16_A	66	CA8_A	102	V_{SS}	138	V_{SS}	174	V_{SS}	210	CA9_A	246	DQ2_B	282	DQS3_B_t
31	V_{SS}	67	CA10_A	103	DQ1_B	139	DQ28_B	175	DQ18_A	211	CA11_A	247	V_{SS}	283	V_{SS}
32	DQ17_A	68	V_{SS}	104	V_{SS}	140	V_{SS}	176	V_{SS}	212	V_{SS}	248	DQ3_B	284	DQ30_B
33	V_{SS}	69	CA12_A	105	DQS0_B_c	141	DQ29_B	177	DQ19_A	213	RFU	249	V_{SS}	285	V_{SS}
34	DQS2_A_c	70	RFU	106	DQS0_B_t	142	V_{SS}	178	V_{SS}	214	RFU	250	DM0_B_n	286	DQ31_B
35	DQS2_A_t	71	V_{SS}	107	V_{SS}	143	RFU	179	DM2_A_n	215	V_{SS}	251	V_{SS}	287	V_{SS}

Pin Assignments (Continued)

288-Pin DDR5 UDIMM Front								288-Pin DDR5 UDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
36	V_{SS}	72	CK0_A_t	108	DQ4_B	144	RFU	180	V_{SS}	216	CK1_A_t	252	DQ6_B	288	RFU

Pin Descriptions

Symbol	Description
CA0_A − CA12_A, CA0_B − CA12_B	SDRAM Command / Address bus
CS0_A_n − CS1_A_n, CS0_B_n − CS1_B_n	SDRAM Chip Select
DQ0_A − DQ31_A, DQ0_B − DQ31_B,	DIMM memory data bus
CB0_A – CB3_A, CB0_B – CB3_B	DIMM ECC check bits
DQS0_A_t – DQS4_A_t, DQS0_B_t – DQS4_B_t	SDRAM data strobes (positive line of differential pair)
DQS0_A_c – DQS4_A_c, DQS0_B_c – DQS4_B_c	SDRAM data strobes (negative line of differential pair)
DM0_A_n – DM3_A_n, DM0_B_n – DM3_B_n	SDRAM data masks
CK0_A_t, CK1_A_t, CK0_B_t, CK1_B_t	SDRAM clocks (positive line of differential pair)
CK0_A_c, CK1_A_c, CK0_B_c, CK1_B_c	SDRAM clocks (negative line of differential pair)

Symbol	Description
HSCL	SidebandBus clock
HSDA	SidebandBus data
HAS	SidebandBus address
ALERT_n	SDRAM ALERT_n
RESET_n	Set DRAMs to a known state
*Vin*_BULK	5V power input supply to the PMIC for analog circuits
Vss	Power supply return (ground)
PWR_GOOD	Power good indicator
PWR_EN	PMIC Enable
RFU	Reserved for future use

Note:
DDR5 UDIMM has 2 channels (channel-A and channel-B) of signal bus.
The signals with suffix:_A (e.g. DQ0_A) are for channel-A, and the signals with suffix:_B (e.g. DQ0_B) are for channel-B

DIMM Voltage Requirements

Symbol	Parameter	Voltage Rating (V)			Maximum Expected Current (A)	Power State
		Min.	TYP.	Max.		
V_{IN}_BULK	Host Supply Voltage	4.25	5.0	5.5	2.5 / 2.0	Operational
SWA, SWB	PMIC Output Supply Voltage	-	1.1	-	6	Operational
SWA+SWB	PMIC Output Supply Voltage	-	1.1	-	12	Operational
SWC	PMIC Output Supply Voltage	-	1.8	-	2	Operational
1.8V LDO	PMIC Output Supply Voltage	-	1.8	-	0.025	Operational
1.0V LDO	PMIC Output Supply Voltage	-	1.0	-	0.020	Operational

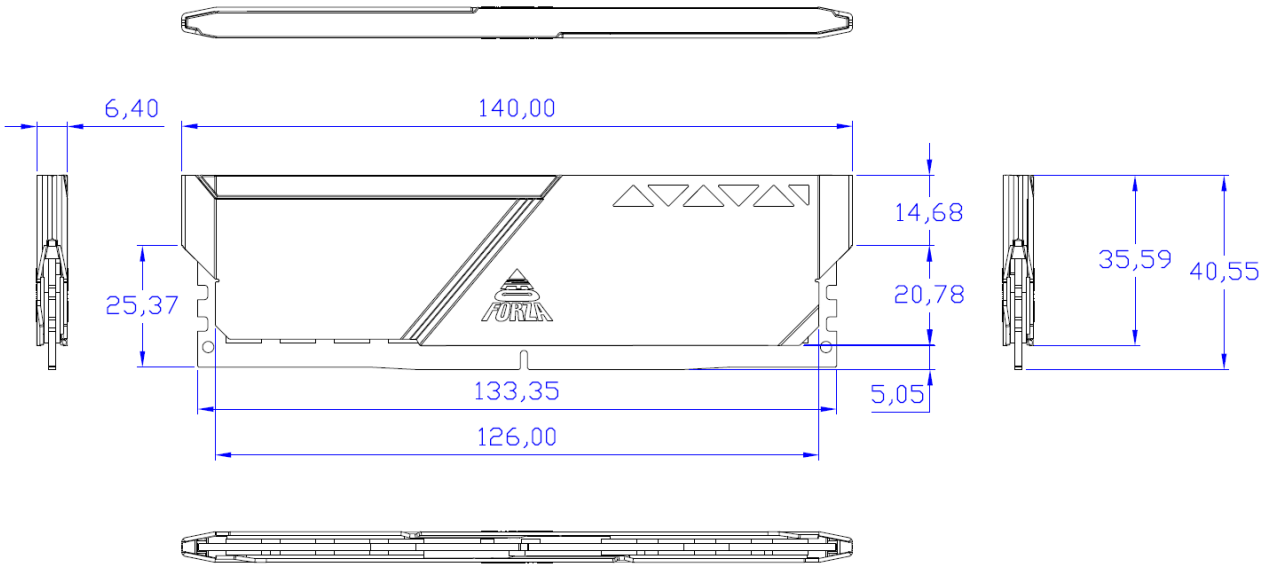
Note:
1. During first power on the input voltage supply must reach minimum 4.25V for PMIC to detect valid input supply.
2. The ramp up rate between 300 mV and 4.0V.
3. The ramp down rate between 4V and 300 mV.
4. The area under the curve above V_{IN}_Bulk = TBD V. V_{IN}_Bulk_AC spec must also be satisfied.
5. The minimum input current requirement is to deliver the maximum output current on V_{OUT}_1.8V and V_{OUT}_1.0V LDO plus the current.
6. V_{IN}_Bulk = 5.0V. Measured at room temperature. All circuitry including output requlators and LDOs are off. VR_EN signal is static.
7. V_{IN}_Bulk = 5.0V. Measured at room temperature. All output requlators and LDOs are on with 0 A output load.. VR_EN signal is static.
8. 20MHz bandwidth limited measurement for all voltage in the table.
9. Voltages are measured at the DIMM gold fingers and at PMIC output pins.
10. The SDRAM specification must be met and take precedence over this document.
11. Maximum current establishes the plaform maximum current regulation point. It provides a data point for DIMM developers ro set power plane impedances.
12. Typical voltage is platform dependent. This is a suggested calue only.
13. Follow JEDEC specification.

Recommended Operating Temperature Ranges

Symbol	Parameter	Rating	Units	Notes
T_{OPR}	Normal Operating Temperature Range	0 ~ 85	°C	1,2
	Extended Temperature Range (Optional)	85 ~ 95	°C	1,3

Note:
1. The operating temperature is the case surface temperature on the center-top side of the DDR5 device. For measurements conditions, refer to JESD51-2.
2. Normal is themaximum limit when device is operationg in the Normal Temperature Mode.
3. Extended is the maximum limit when device is operating in the Extended Temperature Mode.

Physical Dimensions (PCB with Heatsink)



Note: 1. All dimensions are in millimeters; MAX/MIN or typical (TYP) where noted.
2. Tolerance on all dimensions ±0.3 unless otherwise specified.
3.The dimensional diagram is for reference only.

Packing Box

Front side

Back side

Note: The specification stickers on the package are for reference only.

Part Number Decode

N M UD 5 16 F 8 2 – 4800 J A 0 0

Brand
N = Neo Forza

Type Code
M = Module

Module Type
UD = UDIMM
SO = SO-DIMM
RD = RDIMM
ED = ECC UDIMM
ES = ECC SO-DIMM
GD = RGB UDIMM
VR = VLP RDIMM

DRAM Generation
1 = DDR
2 = DDR2
3 = DDR3
4 = DDR4
5 = DDR5

Module Density
12 = 512MB
10 = 1GB
20 = 2GB
40 = 4GB
80 = 8GB
16 = 16GB
24 = 24GB
32 = 32GB
48 = 48GB
64 = 64GB

DRAM Data Depth
A = 64Mb
B = 128Mb
C = 256Mb
D = 512Mb
E = 1Gb
F = 2Gb
G = 4Gb
H = 3Gb

DRAM Data Width
4 = x4
8 = x8
9 = x8 DDP
A = x16

IC Brand

DDR2:
1 = Elpida / Nanya
2 = GK

DDR4:
1 = SK hynix
2 = GK / SK hynix
3 = Micron
4 = Samsung
5 = Nanya
7 = CXMT
8 = SpecTek
9 = SK hynix C-die(OG)
A = SK hynix D-die(OG)
B = Samsung C-die(OG)
C = Samsung F-die(OG)
D = Nanya(OG)
E = SK hynix C-die(ETT)
F = SK hynix D-die(ETT)

DDR5:
1 = SK hynix
2 = GK
3 = Micron
4 = Samsung
5 = Nanya
6 = SK hynix A-die(OG)

Speed
0800 = DDR2-800
1333 = DDR3-1333
1600 = DDR3-1600
2133 = DDR4-2133
213A = DDR4-2133 with Rambus -GS03
2400 = DDR4-2400
240A = DDR4-2400 with Rambus -GS03
2666 = DDR4-2666
266A = DDR4-2666 with Rambus -GS03
293A = DDR4-2933 with Rambus -GS03
3000 = DDR4-3000
3200 = DDR4-3200
320A = DDR4-3200 with Rambus -GS03
3600 = DDR4-3600
3601 = DDR4-3600 (18-22-22-42)
4000 = DDR4-4000
4400 = DDR4-4400
4600 = DDR4-4600
5000 = DDR4-5000
4800 = DDR5-4800
5200 = DDR5-5200
5600 = DDR5-5600
6000 = DDR5-6000
6400 = DDR5-6400
6800 = DDR5-6800
7200 = DDR5-7200
7600 = DDR5-7600
8000 = DDR5-8000
8400 = DDR5-8400
8800 = DDR5-8800

Voltage
A = 2.5V
B = 1.8V
C = 1.5V
D = 1.35V
E = 1.2V
F = 1.4V
G = 1.45V
H = 1.55V
I = 1.6V
J = 1.1V
K = 1.25V
L = 1.3V
M = 1.15V
N = 1.1V (XMP)

Package Code 1
A = Standard without heatsink
B = Faye (Red heatsink)
C = Encke (Golden heatsink)
D = Finlay (Golden heatsink)
E = Mars (Red heatsink)
F = Mars (Gray heatsink)
G = Faye (Black heatsink)
H = Trinity (White heatsink)
I = Trinity (Black heatsink)
J = Trinity (Silver heatsink)
K = Encke (Black heatsink)
L = MDK5

Package Code 2
0 = Industrial Packaging
1 = Single DIMM
2 = Two DIMM Kits
3 = Four DIMM Kits
4 = Eight DIMM Kits

Features Grade
0 = Consumer
C = Quasi Industrial
I = Industrial